Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A method of operating a programmable logic integrated circuit comprising:

loading an initial value in a count register of a watchdog timer circuit of the programmable logic integrated circuit;

clocking the count register to advance the count register to a next value with each clock;

periodically reloading the count register with the initial value;

when the stored count value held in the count register of the watchdog timer circuit reaches a final value, asserting a triggered signal output; and

upon receiving the triggered signal output in a reset logic block of the programmable logic integrated circuit, causing reloading of configuration data from an external source into the programmable logic integrated circuit.

2. (Original) The method of claim 1 wherein the external source is a nonvolatile memory.

3. (Original) The method of claim 1 wherein the external source is a serial EPROM.

4. (Original) The method of claim 1 wherein the final value causes an overflow condition for the count register of the watchdog timer circuit.

5. (Original) The method of claim 1 wherein the watchdog timer circuit increments the stored count value at each clock pulse.

6. (Original) The method of claim 1 wherein the watchdog timer circuit decrements the stored count value at each clock pulse.

7. (Original) The method of claim 1 wherein periodically reloading the count register comprises:

writing a magic value into a reload register of the watchdog timer circuit; and

when the magic value is received in the reload register, resetting the count register of the watchdog timer circuit to the initial value.

8. (Original) The method of claim 1 wherein periodically reloading the count register comprises:

writing a first magic value into a reload register of the watchdog timer circuit;

when the first magic value is received in the reload register, reloading the count register of the watchdog timer circuit to the initial value; and

after the first magic value is received in the reload register, permitting a subsequent reload of the count register when a second magic value is written into reload register.

9. (Original) The method of claim 8 further comprising:

continually reloading the count register to the initial value by writing the first and second magic values to the reload register in sequence, alternately.

10. (Original) The method of claim 1 further comprising:

using the configuration data to configure an embedded processor portion and a programmable logic portion of the programmable logic integrated circuit.

11. (Original) The method of claim 1 wherein to avoid asserting the triggered signal output, a periodic reload of the watchdog timer circuit should be performed during a time period it takes the watchdog timer circuit to count from the initial value to the final value.

12. (Original) The method of claim 11 wherein the period is less than about two minutes.

13. (Original) The method of claim 11 wherein the time period depends on clock frequency used to clock the watchdog timer circuit.

14. (Original) The method of claim 1 wherein the initial value is 0 and the final value is a maximum count value permitted by the count register.

15. (Original) The method of claim 1 wherein the count register comprises 32 bits.

16. - 43. (Canceled).

44. (Original) A method of operating a programmable logic integrated circuit comprising:

clocking a watchdog timer circuit to advance a count register of the watchdog timer circuit;

loading a first magic value into a reload register of the watchdog timer circuit, which resets the count register to an initial value;

after loading the first magic value, loading a second magic value into the reload register, which causes the count register to reset the initial value; and

after loading the first magic value into the reload register, loading a value other than the second magic value into the reload register, which causes the watchdog timer circuit to generate a triggered signal.

45. (Original) The method of claim 44 further comprising:

receiving the triggered signal in a reset logic block of the integrated circuit, which causes a reloading of configuration data from an external source into the integrated circuit.

46. (Original) The method of claim 45 wherein the configuration data is used to configure an embedded processor portion and a programmable logic portion of the integrated circuit.

47. (Original) The method of claim 45 wherein the watchdog timer circuit is located in an embedded processor portion and the reset logic block is located in a programmable logic portion of the integrated circuit.

48. (Original) The method of claim 44 further comprising:

allowing the count register of the watchdog timer to advance to a final value before the first or second magic values are loaded, which causes the watchdog timer circuit to generate the triggered signal.

49. (Original) The method of claim 44 wherein the initial value is 0.

50. (Original) The method of claim 44 wherein the initial value is a value other than 0.

51. (Original) The method of claim 44 wherein the first magic value is different from the second magic value.

52. (Original) The method of claim 48 wherein the final value is user-selectable.

53. (Original) The method of claim 48 wherein the final value is the maximum count permitted by the count register.

54. (Original) The method of claim 44 wherein in a debug mode, the count register does not advance.